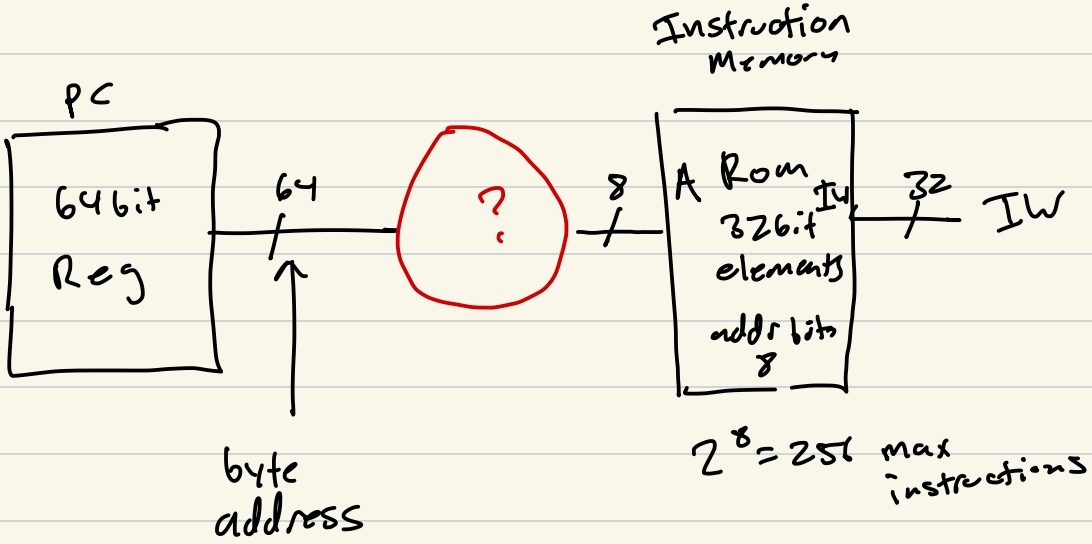
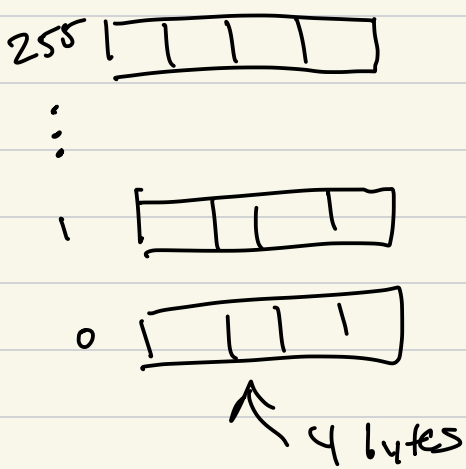
CS315-02 Processor Design Decoding

Lab 05 - RegFile and ALU



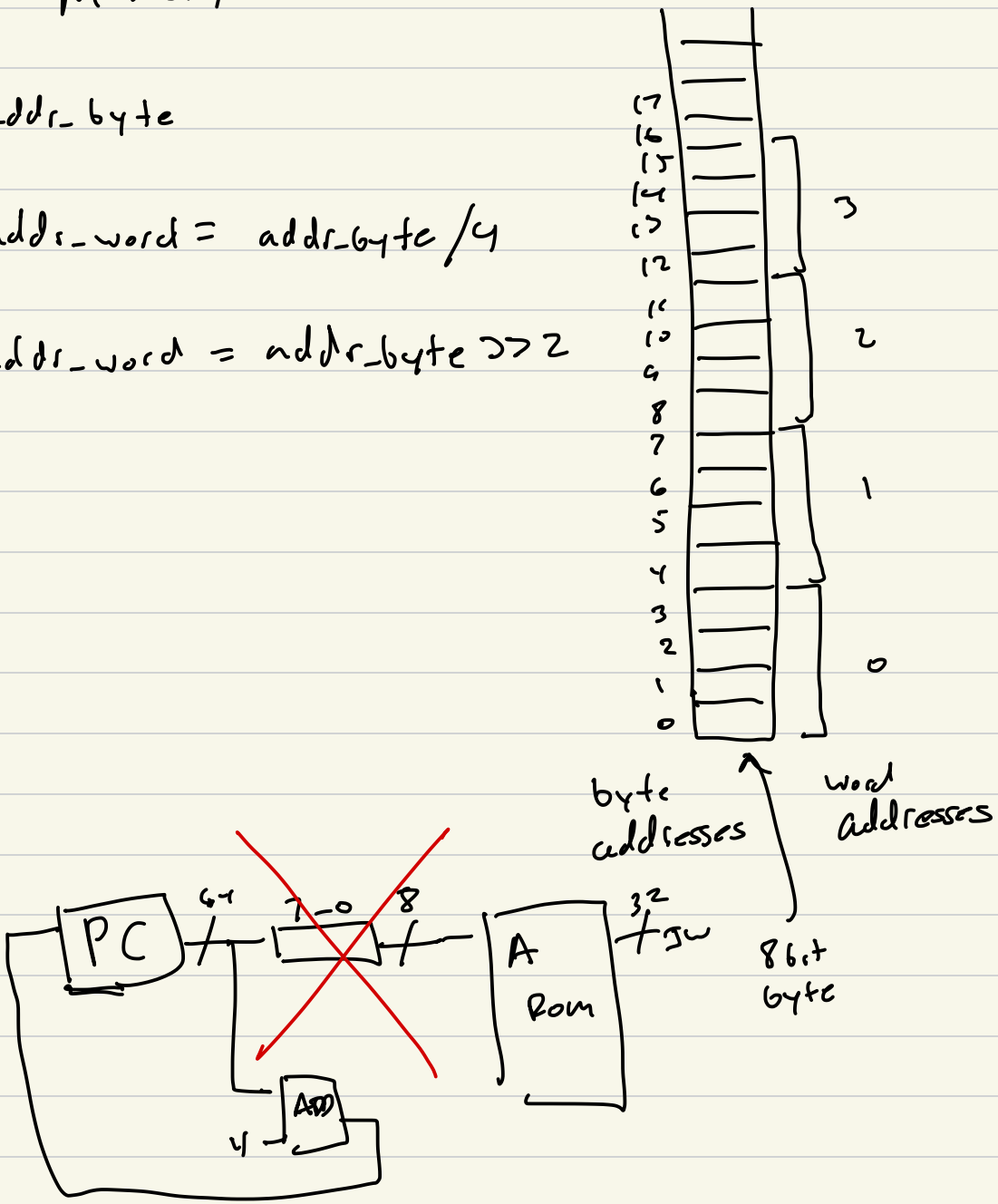


Memory

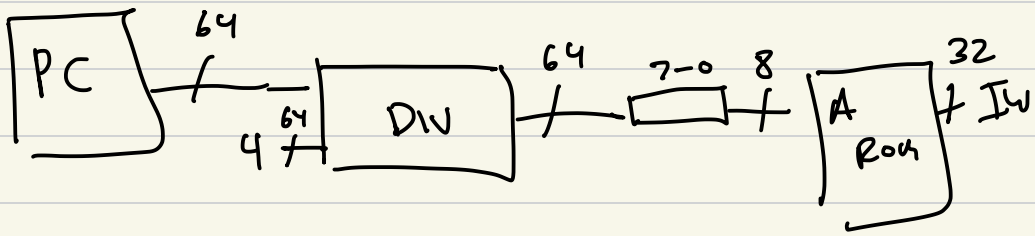
addr_byte

addr_word = addr_byte / 4

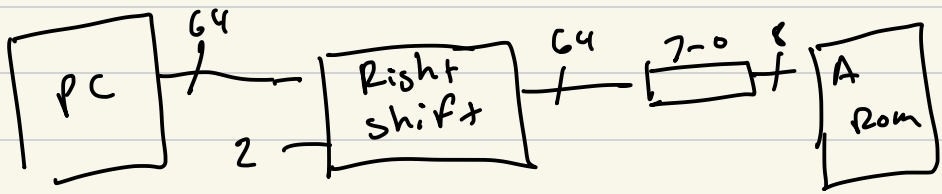
addr_word = addr_byte >> 2



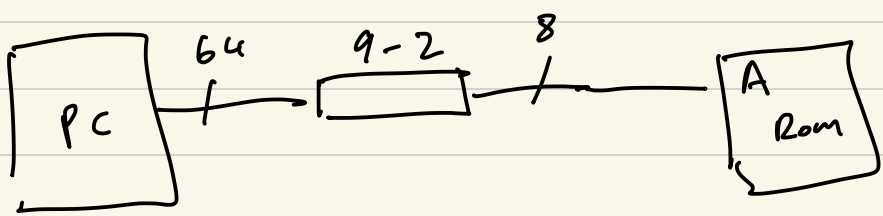
①

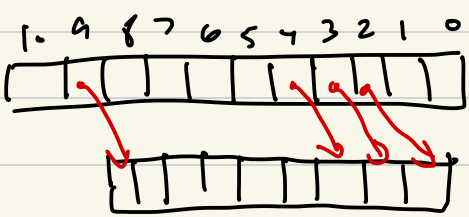

PC
64
64
4
DIV
64
7-0
8
A
Rom
32
IW

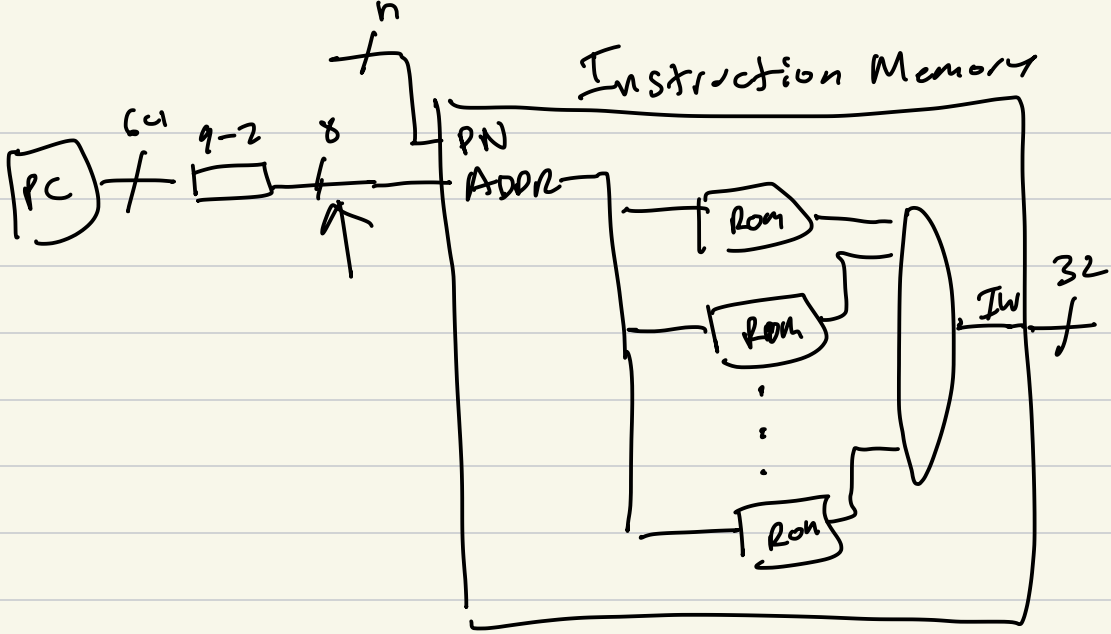
②


PC
64
2
Right shift
64
7-0
8
A
Rom

✱
③


PC
64
9-2
8
A
Rom


10 9 8 7 6 5 4 3 2 1 0

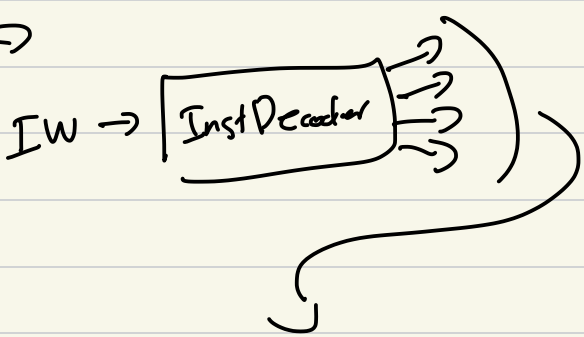


Decoding

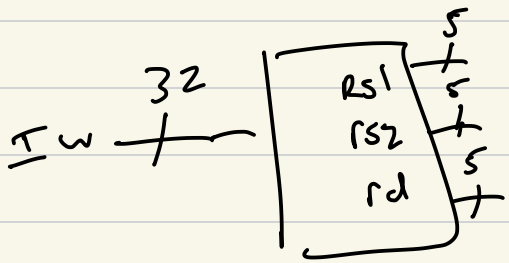
Reg Decoder → get reg #s

Imm Decoder → form a 64 bit signed immediate

Inst Decoder →



Reg Decoder

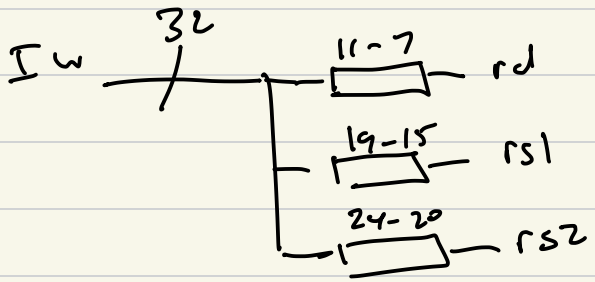


⇒ RegFile

add t0, t1, t2

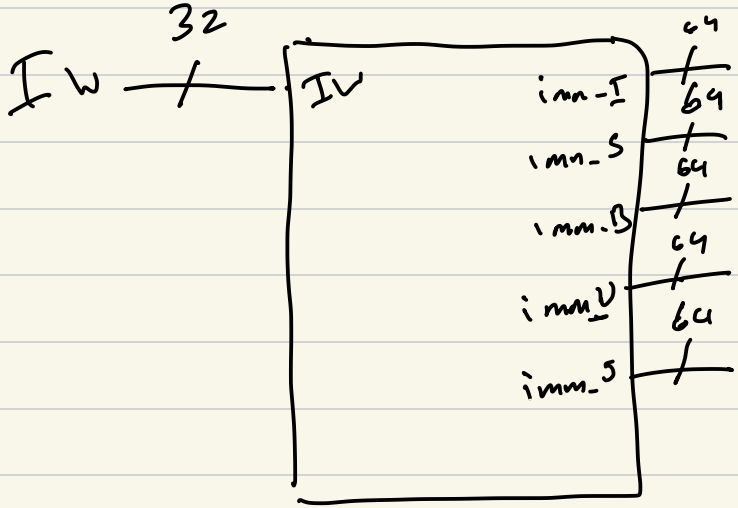
WR RD0 RD1

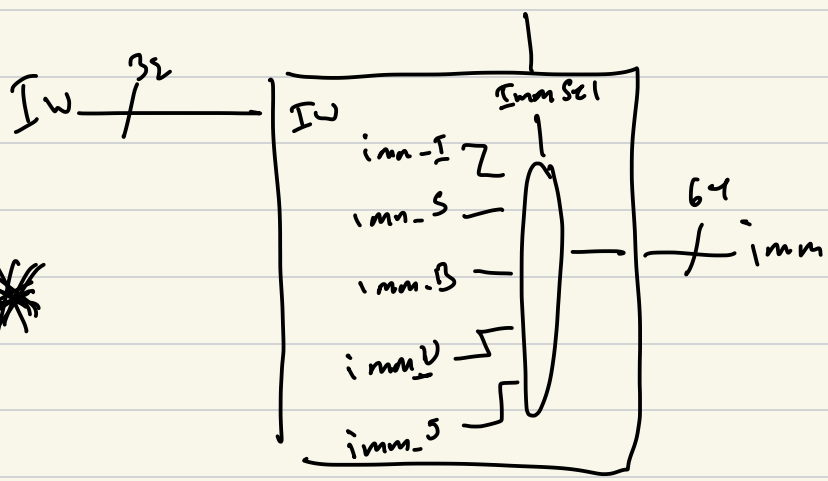
One splitter



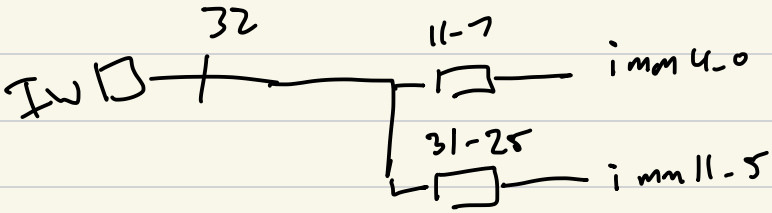
Can choose order of splitter output

Imm Decoder

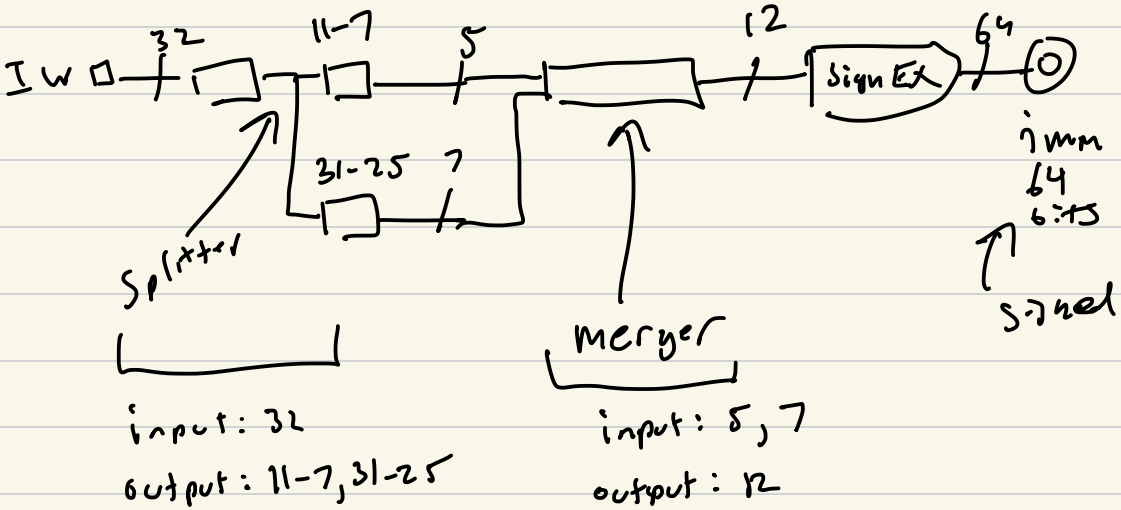

IW
32
IV
imm_I
imm_S
imm_B
imm_U
imm_J
64
64
64
64
64


IW
32
IV
ImmSel
imm_I
imm_S
imm_B
imm_U
imm_J
64
imm

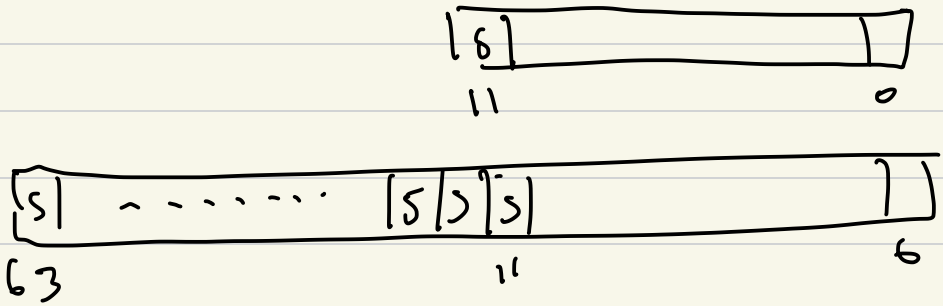
S-Type Immediate



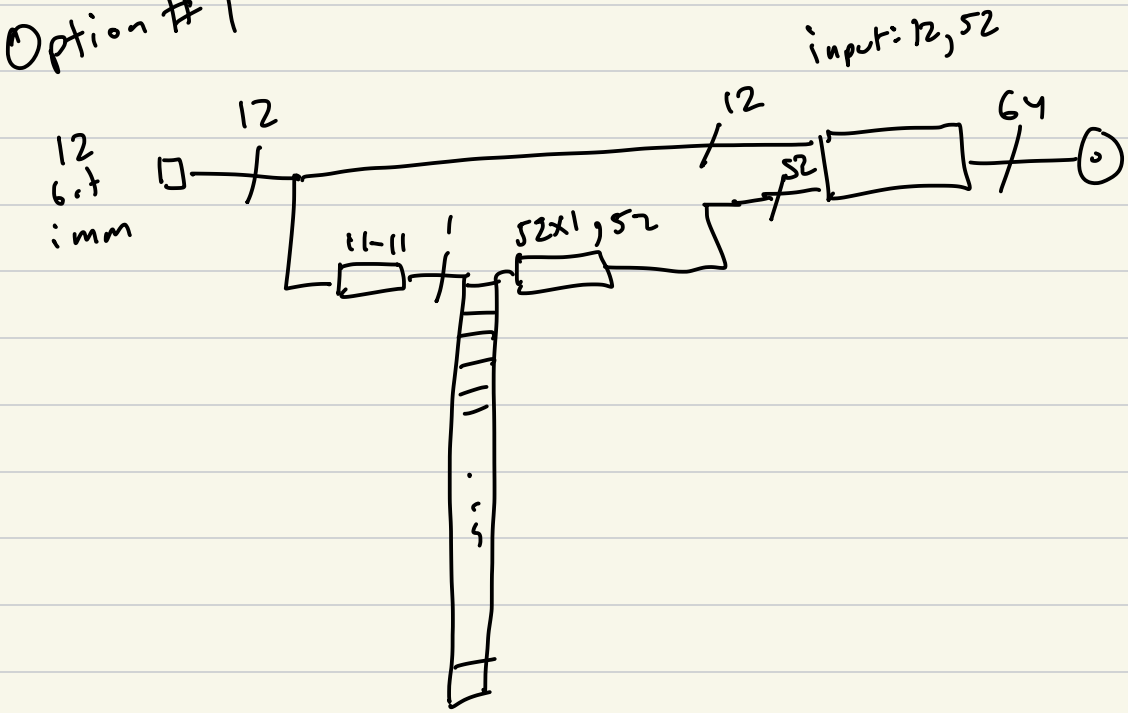
Goal: To construct a 64 bit signed value



How to implement the sign extender



Option #1



Option #2